



TO-247

PRODUCT SUMMARY

V_{DS} (V)

R_{DS(on)} (Ω)

Q_{qs} (nC)

Q_{ad} (nC)

Q_g (Max.) (nC)

Configuration

Power MOSFET

S

N-Channel MOSFET

0.40

500

150

20

80

Single

 $V_{GS} = 10 V$

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP450PbF

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	500		
Gate-Source Voltage			V _{GS}	± 20	- V	
Continuous Drain Current V_{GS} at 10 V $T_C = 25 \degree C$		1	14			
$v_{GS} \text{ at 10 } v_{TC} = 100 \text{ °C}$			ID	8.7	А	
Pulsed Drain Current ^a		I _{DM}	56			
Linear Derating Factor				1.5	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	760	mJ	
Repetitive Avalanche Current ^a			I _{AR}	8.7	А	
Repetitive Avalanche Energy ^a			E _{AR}	19	mJ	
Maximum Power Dissipation	$T_{\rm C} = 2$	25 °C	PD	190	W	
Peak Diode Recovery dV/dt ^c			dV/dt	3.5	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150		
Soldering Recommendations (Peak Temperature) for 10 s				300 ^d	°C	
Mounting Torque	6.20 or M	10.00*014		10	lbf · in	
Mounting Torque	6-32 or M3 screw			1.1	N · m	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 7.0 mH, R_G = 25 Ω , I_{AS} = 14 A (see fig. 12)
- c. $I_{SD} \leq 14$ A, $dI/dt \leq 130$ A/µs, $V_{DD} \leq V_{DS}, \, T_J \leq 150 \ ^\circ C$

d. 1.6 mm from case

1



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SHA)

Vishay Siliconix

Maximum Junction-to-Ambient R _{InJA} - 40 Case-to-Sink, Flat, Greased Surface R _{BOS} 0.24 - 0.65 SPECIFICATIONS T _J = 25 °C, unless otherwise noted SPECIFICATIONS T _J = 25 °C, unless otherwise noted Specific Attions T _J = 25 °C, unless otherwise noted Static Visit Vos Vos Vos Specific Attions Min. TYP. MAX. UNI Gate-Source Treshold Voltage Vos Vos Loss Vos 200 - 4.00 V Gate-Source Leakage I coss Vos Source Con-State Resistance Possen Vos 500 V. Vos 0.01 - - 4.00 V Drain-Source On-State Resistance Possen Vos 500 V. Vos 0.01 - - 2600 - - 2600 - - 2600 - - 2600 - - 2600 - - 2600 - - 2600 - - 720 -	THERMAL RESISTANCE RATI	NGS							
Case-to-Sink, Flat, Greased Surface R_{BLG} 0.24 $ ^{\circ}$ C/W Maximum Junction-to-Case (Drain) R_{BJC} $ 0.65$ $^{\circ}$ C/W SPECIFICATIONS T _J = 25 °C, unless otherwise noted PARAMETER SYMBOL TEST CONDITIONS Min. TYP. MAX. UNI Symmetry Coefficient Algo to the symmetry coefficient Algo to the symmetry coefficient Vogs Temperature Coefficient $\Delta V_{OS} T_J$ Reference to 25 °C, lp = 1 mA $ 0.63$ $ V_{OS}$ Gate-Source Leakage lgss $V_{OS} = V_{OS}$, lp = 250 µA 2.0 $ 4.0$ V Zero Gate Voltage Drain Current lbss $V_{OS} = 10 V$ $V_{OS} = 0 V$, $V_{OS} = 0 V$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$ $ 2.60$	PARAMETER	SYMBOL	TYP.		MAX.			UNIT	
Maximum Junction-to-Case (Drain) $R_{B,LC}$ - 0.65 SPECIFICATIONS $T_J = 25 °C$, unless otherwise noted PARAMETER SYMBOL TEST CONDITIONS MIN. TYP. MAX. UNI Static Drain-Source Breakdown Voltage V_{DS} $V_{CS} = 0 V$, $I_D = 250 \mu A$ 500 - - V/P Gate-Source Threshold Voltage V_{DS} $V_{CS} = 0 V$, $I_D = 14 A$ - 0.63 - 4.0 V/P Case-Source Threshold Voltage V_{DS} $V_{CS} = 0 V$, $I_D = 14 A$, $V_{DS} = 0 V$ - + 100 n^A Zaro Gate Voltage Drain Current I_{DSS} $V_{DS} = 400 V$, $V_{CS} = 0 V$ - - 250 μ^A Drain-Source On-State Resistance $R_{DS(ort)}$ $V_{DS} = 10 V$ $I_D = 8.4 A^D$ 9.3 - - S Dynamic Input Capacitance C_{Case} $V_{DS} = 0 V$, $V_{DS} = 400 V$, $I_D = 8.4 A^D$ - - 0.404 Ω 0.10 1.16 - 2.200 - - 0.404 Ω Drain-Source On-State Resistance C_{DSB} $V_{DS} = 0 V$, $V_{DS} = 0 V$, $V_{DS} = 0 V$, $V_{DS} = $	Maximum Junction-to-Ambient	R _{thJA}	-		40				
SPECIFICATIONS T _J = 25 °C, unless otherwise noted SymBoL TEST CONDITIONS MIN. TYP. MAX. UNI Static Drain-Source Breakdown Voltage V _{DS} V _{DS} = 0, V, I _D = 250 µA 500 - V Static Drain-Source Breakdown Voltage V _{DS} V _{GS} = 0, V, I _D = 250 µA 2.0 - 4.0 V Gate-Source Leakage I/A/DS V _{DS} = 400 V, V _{OS} = 0 V - - 2.4.0 V Calce Source Leakage I/A/DS V _{DS} = 500 V, V _{OS} = 0 V - - 2.50 µA Source Leakage I/A/DS V _{DS} = 10 V I _D = 8.4 A ^b - - 0.40 Ω Parameter Cargacitance Cress V _{DS} = 50 V, I _D = 8.4 A ^b 9.3 - - 0.40 Ω Proving Transconductance Q _{DS} V _{DS} = 10 V I _D = 8.4 A ^b 9.3 - - 0.40 Ω Calce Source Chasse Tran	Case-to-Sink, Flat, Greased Surface	R _{thCS}					°C/W		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Maximum Junction-to-Case (Drain)	R _{thJC}							
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$									
Static VDS VGS = 0 V, ID = 250 µA 500 - - V Orain-Source Breakdown Voltage $\Delta D_{DS}/T_J$ Reference to 25 °C, ID = 1 mA - 0.63 - V/* Gate-Source Threshold Voltage V_{OS} ($S_{S(th)}$ $V_{DS} = V_{GS}$, ID = 250 µA 2.0 - 4.0 V Gate-Source Leakage IcSS $V_{OS} = 20$ V - - ± 100 nA Zero Gate Voltage Drain Current IDSS $V_{OS} = 500$ V, $V_{OS} = 0$ V - - 250 µA Forward Transconductance $R_{S(on)}$ $V_{OS} = 10$ V ID = 8.4 A ^D - - 0.400 Ω Dynamic Input Capacitance C_{css} $V_{DS} = 20$ V, $V_{DS} = 25$ V, $I_D = 8.4$ A ^D 9.3 - 0.400 Ω Dynamic Input Capacitance C_{css} $V_{DS} = 20$ V, $V_{CS} = 20$ V - - 100 10 10 </td <td>SPECIFICATIONS $T_J = 25 \text{ °C}$, u</td> <td>nless otherwi</td> <td>se noted</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	SPECIFICATIONS $T_J = 25 \text{ °C}$, u	nless otherwi	se noted						
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	PARAMETER	SYMBOL	TEST	CONDITI	ONS	MIN.	TYP.	MAX.	UNIT
	Static						•	•	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 28	50 µA	500	-	-	V
	V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I	_D = 1 mA	-	0.63	-	V/°C
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	′ _{GS} , I _D = 2	50 µA	2.0	-	4.0	V
Zero Gate Voltage Drain Current IDSS VDS = 400 V, VGS = 0 V, TJ = 125 °C - - 250 µµ Drain-Source On-State Resistance RDS(on) VGS = 10 V Ib = 8.4 Ab - - 0.40 Q Forward Transconductance gfs VDS = 50 V, Ib = 8.4 Ab 9.3 - - S Dynamic Input Capacitance Ciss VGS = 0 V,	Gate-Source Leakage		V _G	_S = ± 20 \	/	-	-	± 100	nA
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			V _{DS} = 5	00 V, V _{GS}	= 0 V	-	-	25	•
Forward Transconductance g_{fs} $V_{DS} = 50 V$, $I_D = 8.4 A^b$ 9.3 $-$ S Dynamic Input Capacitance C_{iss} $V_{GS} = 0 V$, $V_{DS} = 25 V$, $f = 1.0 MHz$, see fig. 5 $ 720$ $ 7200$ <td>Zero Gate Voltage Drain Current</td> <td>IDSS</td> <td>V_{DS} = 400 V, V</td> <td>/_{GS} = 0 V,</td> <td>T_J = 125 °C</td> <td>-</td> <td>-</td> <td>250</td> <td>μΑ</td>	Zero Gate Voltage Drain Current	IDSS	V _{DS} = 400 V, V	/ _{GS} = 0 V,	T _J = 125 °C	-	-	250	μΑ
DynamicInput Capacitance C_{iss} $V_{GS} = 0 V$, $V_{DS} = 25 V$, $f = 1.0 MHz$, see fig. 5 $ 2600$ $-$ Output Capacitance C_{rss} $f = 1.0 MHz$, see fig. 5 $ 720$ $-$ Reverse Transfer Capacitance C_{rss} $f = 1.0 MHz$, see fig. 5 $ 720$ $-$ Total Gate Charge Q_{g} Q_{gs} $V_{GS} = 10 V$ $I_D = 14 A, V_{DS} = 400 V$, see fig. 6 and 13b $ 150$ Gate-Drain Charge Q_{gd} $V_{GS} = 10 V$ $I_D = 14 A, V_{DS} = 400 V$, see fig. 6 and 13b $ 80$ Turn-On Delay Time $t_{d(on)}$ $V_{GS} = 10 V$ $V_{DD} = 250 V, I_D = 14 A,$ $R_G = 6.2 \Omega, R_D = 17 \Omega$, see fig. 10^{b} $ 44$ Turn-Off Delay Time $t_{d(off)}$ $R_G = 6.2 \Omega, R_D = 17 \Omega$, see fig. 10^{b} $ 44$ $-$ Internal Drain Inductance L_D Between lead, $6 mm (0.25^{a}) frompackage and center ofdie contact 5.0-Drain-Source Body Diode Characteristics 14-Pulsed Diode Forward CurrentI_SMOSFET symbolshowing theintegral reversep - n junction diode 14-Body Diode Reverse Recovery Timet_{rr}T_J = 25 °C, I_F = 14 A, dl/dt = 100 A/\mu s^b 4.87.2\mu C$	Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D	= 8.4 A ^b	-	-	0.40	Ω
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Forward Transconductance	g _{fs}	V _{DS} = 5	0 V, I _D = 8	3.4 A ^b	9.3	-	-	S
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Dynamic								
Output Capacitance C_{oss} $V_{DS} = 25 \text{ V}$, f = 1.0 MHz, see fig. 5-720-pFReverse Transfer Capacitance C_{rss} $f = 1.0 \text{ MHz}$, see fig. 5-720-pFReverse Transfer Capacitance C_{rss} $f = 1.0 \text{ MHz}$, see fig. 5-340Total Gate Charge Q_g Gate-Source Charge Q_{gd} $V_{GS} = 10 \text{ V}$ $I_D = 14 \text{ A}$, $V_{DS} = 400 \text{ V}$, see fig. 6 and 13b20nCGate-Drain Charge Q_{gd} $V_{GS} = 10 \text{ V}$ $I_D = 14 \text{ A}$, $V_{DS} = 400 \text{ V}$, see fig. 6 and 13b80Turn-On Delay Time $t_{d(on)}$ $V_{GS} = 6.2 \Omega$, $R_D = 17 \Omega$, see fig. 10b47Turn-Off Delay Time $t_{d(off)}$ $R_G = 6.2 \Omega$, $R_D = 17 \Omega$, see fig. 10b-44Internal Drain Inductance L_D Between lead, 6 mm (0.25") from package and center of die contact-5.0Internal Source Inductance L_S MOSFET symbol showing the integral reverse p - n junction diode14Pulsed Diode Forward Current* I_S N_{SD} $T_J = 25 \text{ °C}$, $I_F = 14 \text{ A}$, $dI/dt = 100 \text{ A/µsb}$ 1.4VBody Diode Reverse Recovery Charge Q_{rr} $T_J = 25 \text{ °C}$, $I_F = 14 \text{ A}$, $dI/dt = 100 \text{ A/µsb}$ 4.87.2 μ C	Input Capacitance	C _{iss}	$V_{\rm DS} = 25$ V,		-	2600	-	pF	
Reverse Iranster Capacitance C_{rss} -340-Total Gate Charge Q_g Gate-Source Charge Q_{gs} Gate-Drain Charge Q_{gd} Turn-On Delay Time $t_{d(on)}$ Rise Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_r Internal Drain Inductance L_D Between lead, 6 mm (0.25°) from package and center of die contactInternal Source Inductance L_S MOSFET symbol showing the integral reverse $p - n$ junction diodePulsed Diode Forward Currenta I_S Body Diode Voltage V_{SD} Turn-Spice Recovery Time t_{rr} Turn-Spice Recovery Charge Q_{rr} Turn-Spice Recovery Charge $Q_$	Output Capacitance	C _{oss}			-	720	-		
$ \begin{array}{c c c c c c c } \hline Total Gate Charge & Q_g & \\ \hline Gate-Source Charge & Q_{gs} & \\ \hline Gate-Drain Charge & Q_{gd} & \\ \hline U_{GS} = 10 \ V & \\ \hline V_{GS} = 10 \ V & \\ \hline I_{D} = 14 \ A, \ V_{DS} = 400 \ V, \\ \hline see \ fig. \ 6 \ and \ 13^{D} & \hline & - & 20 & \\ \hline - & - & 80 & \\ \hline & - & - & 80 & \\ \hline & - & - & 80 & \\ \hline & - & - & 80 & \\ \hline & - & - & 80 & \\ \hline & - & - & 80 & \\ \hline & - & - & 80 & \\ \hline & - & - & 17 & - & \\ \hline & - & 47 & - & \\ \hline & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & 44 & - & \\ \hline & - & - & - & - & 14 & \\ \hline & - & - & 13 & - & \\ \hline & - & - & 14 & \\ \hline & - & - & - & 14 & \\ \hline & - & - & - & - & 14 & \\ \hline & - & - & - & - & 14 & \\ \hline & - & - & - & - & - & 14 & \\ \hline & - & - & - & - & - & - & - & 14 & \\ \hline & - & - & - & - & - & - & - & - & - &$	Reverse Transfer Capacitance	C _{rss}			-	340	-		
Gate-Source Charge d_{gs} $V_{GS} = 10$ $^{\circ}$ see fig. 6 and 13b $^{\circ}$ <td>Total Gate Charge</td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td>-</td> <td>150</td> <td></td>	Total Gate Charge					-	-	150	
Gate-Drain Charge Q_{gd} $ 80$ Turn-On Delay Time $t_{d(on)}$ Rise Time t_r Turn-Off Delay Time $t_{d(off)}$ Fall Time t_f Fall Time t_f Internal Drain Inductance L_D Internal Source Inductance L_S Drain-Source Body Diode CharacteristicsContinuous Source-Drain Diode CurrentIsMOSFET symbol showing the integral reverse $p - n$ junction diodePulsed Diode Forward CurrentaIsMost Source Recovery Time t_r Turn-Off Delay Time t_r Turn-Off Delay Time $T_J = 25 ^\circ C$, $I_S = 14 A$, $V_{GS} = 0 V^b$ $r = 14 A$, $dI/dt = 100 A/\mu s^b$ $ r = 14 A$, $T_r = 14 A$, $dI/dt = 100 A/\mu s^b$ $r = 14 A$, $T_r = 14$	Gate-Source Charge	Q _{gs}	V _{GS} = 10 V			-	-	20	nC
Rise Time t_r $V_{DD} = 250 \text{ V}, \text{ I}_D = 14 \text{ A}, \text{ R}_G = 6.2 \Omega, \text{ R}_D = 17 \Omega, \text{ see fig. 10^b}$ $ 47$ $ 92$ $ 44$ $ 92$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ -$ <	Gate-Drain Charge			300 11	g. o and to	-	-	80	
Rise Time t_r $V_{DD} = 250 \text{ V}, \text{ I}_D = 14 \text{ A}, \text{ R}_G = 6.2 \Omega, \text{ R}_D = 17 \Omega, \text{ see fig. 10^b}$ $ 47$ $ 92$ $ 44$ $ 92$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ 44$ $ -$ <	Turn-On Delay Time	t _{d(on)}				-	17	-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Rise Time		- V 2	50 V I	1/Δ	-	47	-	
Fall Time t_f -44-Internal Drain Inductance L_D Between lead, 6 mm (0.25") from package and center of die contact-5.0-Internal Source Inductance L_S Between lead, 	Turn-Off Delay Time	t _{d(off)}	$R_{\rm G} = 6.2 \ \Omega, R_{\rm H}$	$b_{\rm D} = 17 \ \Omega,$	see fig. 10 ^b	-	92	-	ns
Internal Drain HuddetanceLp6 mm (0.25") from package and center of die contact-3.0nInternal Source InductanceLs6 mm (0.25") from package and center of die contact-13-nDrain-Source Body Diode CharacteristicsMOSFET symbol showing the integral reverse p - n junction diode-14APulsed Diode Forward CurrentaIsMOSFET symbol showing the integral reverse p - n junction diode14ABody Diode VoltageV_SDT_J = 25 °C, I_S = 14 A, V_{GS} = 0 V^b1.4VBody Diode Reverse Recovery TimetrrT_J = 25 °C, I_F = 14 A, dI/dt = 100 A/µs^b-540810nsContinuous Cource ChargeQrrContinue ChargeContinue	Fall Time					-	44	-	
Internal Source InductanceLSpackage and center of die contact-13-Drain-Source Body Diode CharacteristicsContinuous Source-Drain Diode CurrentISMOSFET symbol showing the integral reverse p - n junction diode14APulsed Diode Forward CurrentaISMTJ = 25 °C, IS = 14 A, VGS = 0 Vb56ABody Diode Reverse Recovery TimetrrTJ = 25 °C, IS = 14 A, dI/dt = 100 A/µsb-540810nsBody Diode Reverse Recovery ChargeQrrTJ = 25 °C, IF = 14 A, dI/dt = 100 A/µsb-540810ns	Internal Drain Inductance	L _D		m		-	5.0	-	
Continuous Source-Drain Diode CurrentIsMOSFET symbol showing the integral reverse p - n junction diode-14APulsed Diode Forward CurrentaIsMIsMT_J = 25 °C, I_S = 14 A, V_{GS} = 0 V^b56Body Diode VoltageV_{SD}T_J = 25 °C, I_S = 14 A, V_{GS} = 0 V^b1.4VBody Diode Reverse Recovery Time t_{rr} $T_J = 25 °C, I_F = 14 A, dI/dt = 100 A/\mu s^b$ -540810nsBody Diode Reverse Recovery Charge Q_{rr} 4.87.2 μC	Internal Source Inductance	L _S		nter of		-	13	-	
Continuous Source-Drain Diode CurrentIs is showing the integral reverse p - n junction diodeshowing the integral reverse p - n junction diode14APulsed Diode Forward CurrentaIs Is MIs P - n junction diodeIs P - n junction diode14ABody Diode VoltageVsDTJ = 25 °C, Is = 14 A, VGS = 0 Vb1.4VBody Diode Reverse Recovery Timetrr TJ = 25 °C, IF = 14 A, dI/dt = 100 A/µsb-540810ns-4.87.2µC1.4V	Drain-Source Body Diode Characteristic	s							
Pulsed Diode Forward Currenta I_{SM} Integral reverse p - n junction diode $ 56$ Body Diode Voltage V_{SD} $T_J = 25 \ ^{\circ}C$, $I_S = 14 \ A$, $V_{GS} = 0 \ V^b$ $ 1.4 \ V$ Body Diode Reverse Recovery Time t_{rr} $T_J = 25 \ ^{\circ}C$, $I_F = 14 \ A$, $dI/dt = 100 \ A/\mu s^b$ $ 540 \ 810 \ ns$ Body Diode Reverse Recovery Charge Q_{rr} $T_J = 25 \ ^{\circ}C$, $I_F = 14 \ A$, $dI/dt = 100 \ A/\mu s^b$ $ 4.8 \ 7.2 \ \mu C$	Continuous Source-Drain Diode Current	I _S	showing the	bl		-	-	14	
Body Diode Reverse Recovery Time t_{rr} $T_J = 25 \ ^{\circ}C$, $I_F = 14 \ A$, $dI/dt = 100 \ A/\mu s^b$ -540810nsBody Diode Reverse Recovery Charge Q_{rr} $T_J = 25 \ ^{\circ}C$, $I_F = 14 \ A$, $dI/dt = 100 \ A/\mu s^b$ -4.87.2 μC	Pulsed Diode Forward Current ^a	I _{SM}		ode		-	-	56	
$T_{J} = 25 \text{ °C}, I_{F} = 14 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}^{b}$ Body Diode Reverse Recovery Charge Q_{rr} $- 4.8 7.2 \mu\text{C}$	Body Diode Voltage	V _{SD}	T _J = 25 °C, I	_S = 14 A, '	V _{GS} = 0 V ^b	-	-	1.4	V
Body Diode Reverse Recovery Charge Q _{rr} - 4.8 7.2 µC	Body Diode Reverse Recovery Time	t _{rr}	T _ 25 °C	-/الم 1/ ۸	H - 100 4 /	-	540	810	ns
Forward Turn-On Time ton Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)	Body Diode Reverse Recovery Charge	Q _{rr}	$I_{\rm J} = 25 {}^{-}$ U, $I_{\rm F} =$	14 A, al/c	$a = 100 \text{ A/} \mu \text{s}^{5}$	-	4.8	7.2	μC
	Forward Turn-On Time	t _{on}	Intrinsic turn	-on time i	s negligible (turn	on is do	minated b	by L _S and	L _D)

Notes

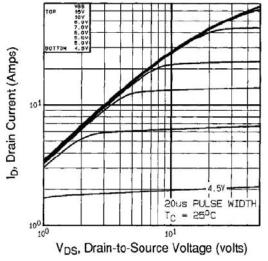
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %

2



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





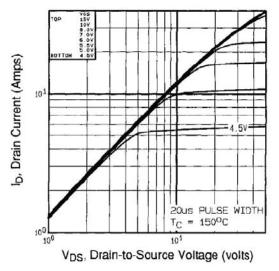


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

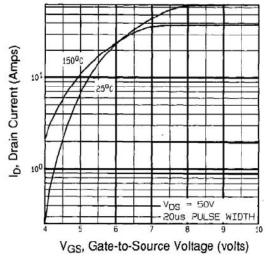


Fig. 3 - Typical Transfer Characteristics

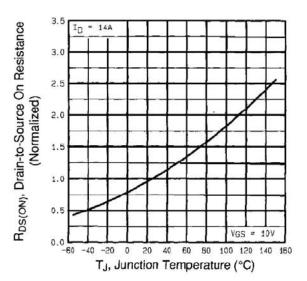


Fig. 4 - Normalized On-Resistance vs. Temperature



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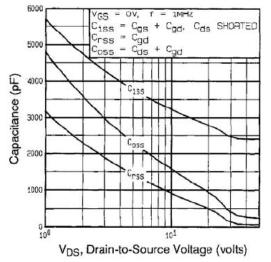


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

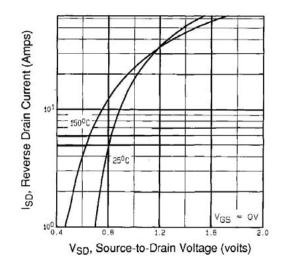


Fig. 7 - Typical Source-Drain Diode Forward Voltage

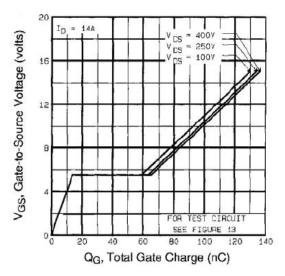


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

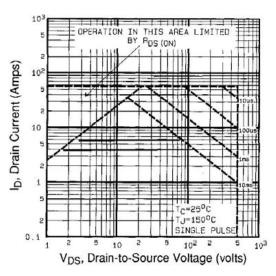


Fig. 8 - Maximum Safe Operating Area



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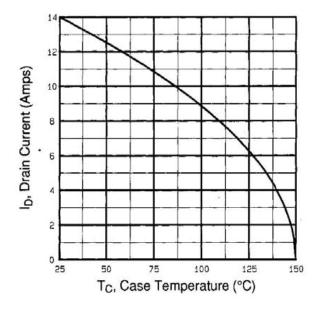


Fig. 9 - Maximum Drain Current vs. Case Temperature

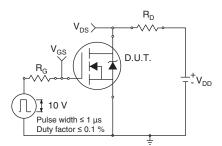


Fig. 10a - Switching Time Test Circuit

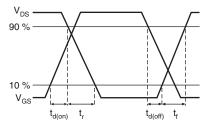
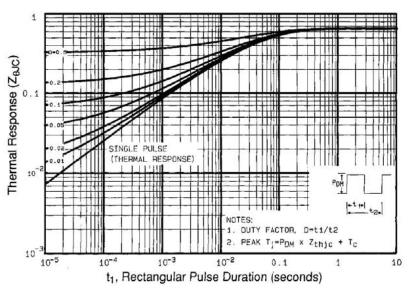
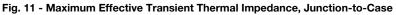


Fig. 10b - Switching Time Waveforms





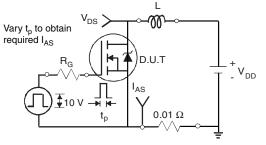


Fig. 12a - Unclamped Inductive Test Circuit

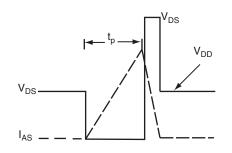


Fig. 12b - Unclamped Inductive Waveforms

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Document Number: 91233

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IRFP450





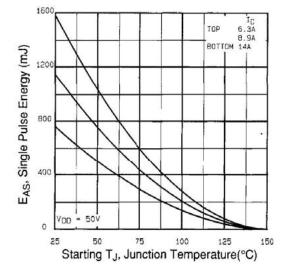


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

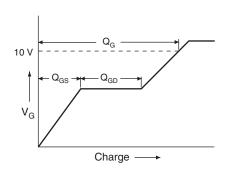


Fig. 13a - Basic Gate Charge Waveform

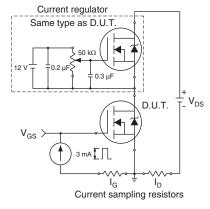
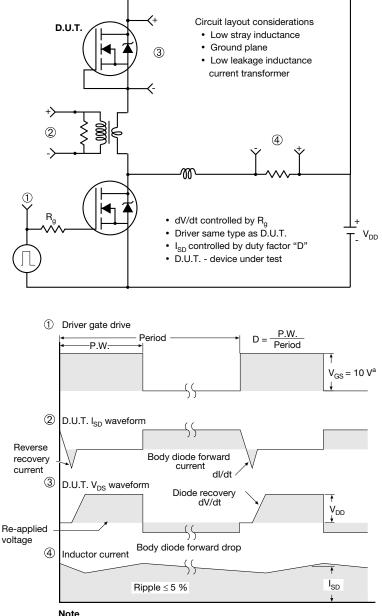


Fig. 13b - Gate Charge Test Circuit





Peak Diode Recovery dV/dt Test Circuit



a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9





Section C--C, D--D, E--E

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
А	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØP	3.56	3.65	7
Ø P1	7.19) ref.	
Q	5.31	5.69	
S	5.54	5.74	

Notes

- ⁽¹⁾ Package reference: JEDEC[®] TO247, variation AC
- (2) All dimensions are in mm
- ⁽³⁾ Slot required, notch may be rounded
- ⁽⁴⁾ Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁵⁾ Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

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VERSION 2: FACILITY CODE = Y



	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
с	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØΡ	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51	BSC	

Notes

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- ⁽²⁾ Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1
- ⁽⁵⁾ Lead finish uncontrolled in L1
- ⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- ⁽⁷⁾ Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



	MILLIN	IETERS		MILLIN	IETERS
DIM.	MIN.	MAX.	DIM.	MIN.	MAX.
А	4.65	5.31	D2	0.51	1.35
A1	2.21	2.59	E	15.29	15.87
A2	1.17	1.37	E1	13.46	-
b	0.99	1.40	е	5.46	BSC
b1	0.99	1.35	k	0.:	254
b2	1.65	2.39	L	14.20	16.10
b3	1.65	2.34	L1	3.71	4.29
b4	2.59	3.43	N	7.62	BSC
b5	2.59	3.38	Р	3.56	3.66
С	0.38	0.89	P1	-	7.39
c1	0.38	0.84	Q	5.31	5.69
D	19.71	20.70	R	4.52	5.49
D1	13.08	-	S	5.51	BSC

Notes

⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994

⁽²⁾ Contour of slot optional

(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1

⁽⁵⁾ Lead finish uncontrolled in L1

⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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